SPECIFICATION AMENDMENTS:

Please amend the specification as follows:

Page 8, line 25, through Page 9, line 3, please amend the current paragraph as follows:

--A mode for carrying out the invention will be described hereinafter, made with reference to the drawings. A same reference number is used for description of what has substantially the same function through the whole drawings and its description will be omitted in some cases.

Page 9, line 6, through line 16, please amend the current paragraph as follows:

In this embodiment, as shown in FIG. 1A, a semiconductor substrate 12 ~~in~~ on which an SOI film 16 (a silicon film) whose thickness is 250 nm, for example, is piled through a medium of a box oxide film 14 (a buried oxide film) (referred to as an SOI substrate 10, hereinafter) is first prepared. A thermal oxide film 18 (a first insulation film) ~~of~~ having a thickness of 300 nm, for example, is formed on the SOI film 16, and a nitride film 20 whose thickness is thinner than the thermal oxide film 18, that is, 10 nm, for example, is further formed on the thermal oxide film 18 by means of a CVD method. A photolithography process and an etching process are carried out to eliminate the thermal oxide film 18 and the nitride film 20 so that a portion to be a channel region of the SOI film 16 would be exposed, and thereby, an opening pattern 22 is formed.--

Page 9, line 21, through Page 11, line 15, please amend the current paragraphs as follows:

--Next, as shown in FIG. 1B, the thermal oxide film 18 and the nitride film 20 are used as a mask to carry out a thermal oxidation process for the exposed portion of the SOI film 16 so as to form a thermal oxide film (a silicon oxide film) 26 having a thickness equal to 100 nm, for example, while ~~make~~ making the channel region of the SOI film 16 thinner. Accordingly, the SOI film 16 has different ~~thickness~~ thicknesses of 50 nm and 100 nm, for example, between its channel region (a region in which a gate electrode is formed) and other regions (a diffusion layer: source and drain regions). That is to say, the thickness of the channel region of the SOI film 16 becomes thinner than that of other regions. Thinning the channel region of the SOI film 16 as described above allows a short channel effect to be restrained.

As shown in FIG. 1C, a wet etching process using 1% hydrofluoric acid ~~of 1%~~, for example, is then carried out for 18 minutes to eliminate a thermal oxide film 26 so that the SOI film 16 would be exposed again. The exposed portion of the SOI film 16 undergoes a thermal oxidation process to form a gate oxide film (a gate insulation film: a third insulation film) 28 having a thickness of 10 nm, for example. A channel ion, a B ion, for example, is implanted in an interface between the SOI film 16 and the gate oxide film 28 by means of an ion implantation method to form a channel region 30. And then, a poly-silicon is deposited over the whole surface so as to fill the opening pattern 22 by means of a CVD method, for example, to form a poly-silicon film 32 having a thickness of 400 nm, for example.

Next, as shown in FIG. 1D, an etching back method or a CMP (chemical and mechanical polishing) method, for example, is used for smoothing the surface while eliminating an unnecessary poly-silicon film 32 formed on the nitride film 20, so that a gate electrode 34 consisting of poly-silicon would be formed inside the opening pattern 22 so as to self align. The nitride film 20 is here eliminated together with an unnecessary poly-silicon film 32 thereon since it is thin, such as 10 nm in thickness.

As shown in FIG. 1E, a wet etching process using hydrofluoric acid of 5%, for example, is then carried out for 10 minutes to eliminate a thermal oxide film 18. Sidewalls 24 ~~respectively~~ comprising a nitride film (SiN), and the thermal oxide film 18 (SiO_2) ~~and a nitride film (SiN)~~ have ~~a~~ different etching selection ~~ratio~~ ratios, respectively. Concretely, SiO_2 has an etching selection ratio that is faster than SiN. Thus, the sidewall 24 comprising a nitride film (SiN) ~~is remained~~ remains while the thermal oxide film 18 is eliminated, so that a gate electrode 34 provided on its side wall with the sidewall 24 would be formed.

Then, as shown in FIG. 1F, the gate electrode 34 is used as a mask to ion-implant (impurity-implant) arsenic in the SOI film 16 surrounding the gate electrode 34 under a condition of an implantation angle of 30 degrees, 50 KeV and 5×10^{15} ions/cm^2, for example. After that, an activation annealing process is carried out at 1000 degrees centigrade, for example, so as to form a source region 36 and a drain region 38 as a diffusion layer so that they would self align. Ti, for example, is then sputtered on surfaces of the gate electrode 34, the source region 36 and the drain region 38 so as to carry out a salicide process, so that a gate silicide region 34a, a source silicide region 36a and a drain silicide region 38a would be respectively formed.--

Page 12, line 2, through line 9, please amend the current paragraph as follows:

--In this embodiment, the sidewall 24 is formed on the inner wall of the opening pattern 22 of the thermal oxide film 18 to form the gate electrode 34 in the opening pattern 22, and then, a difference of an etching selection ratio is utilized to ~~remain~~ keep the sidewall 24, on one hand, while ~~to eliminate~~ eliminating the thermal oxide film 18, on the other hand. That is to say, the gate electrode 34 and the sidewall 24 on a side wall thereof are formed in one process. Accordingly, a process for forming the sidewall 24, which has been separately required conventionally, can be omitted, and thereby, a lower cost can be achieved.--

Page 12, line 14, through Page 13, line 7, please amend the current paragraphs as follows:

--In this embodiment, a nitride film highly resistant to oxidation is used as the sidewall 24 formed on the inner wall of the opening pattern 22 of the thermal oxide film 18. Thus, in a thermal oxidation process for thinning the SOI film 16 or forming the gate oxide film 28, oxidation in a lateral direction of an exposed portion of the SOI film 16 is restrained while that of a downward direction is accelerated. This can more effectively prevent a region of the SOI film other than the channel region from being excessively thinned. Moreover, this makes the difference in size conversion due to oxidation small, which allows an oxide film to be formed into an almost equal size as the opening pattern 22. Accordingly, the gate electrode 34 can be formed with good accuracy in

size even when its pattern is fine, and miniaturization of a device also can be achieved as a whole.

In this embodiment, the nitride film 20 highly resistant to oxidation is further formed on the thermal oxide film 18 as a mask in respective oxidation processes, so that oxidation of a region other than a portion of the SOI film 16 exposed by means of the opening pattern 22 can be further prevented ~~further surely~~.

It goes without saying that a method of manufacturing a semiconductor device of the invention according to the above ~~any~~ embodiment is not construed restrictively but can be achieved in a scope of satisfying requirements of the invention.--